Amendments to the Specification:

Please replace the paragraph beginning on page 7, line 2, with the following amended paragraph:

--The present invention will be more fully explained hereafter with the aid of the drawings which show the following:

Fig. 1, a wiring symbol for an 8-bit adder;

Fig. 2, a wiring symbol for an 8-bit adder according to Fig. 1 consisting of eight 1-bit adders;

Fig. 3, a logical structure of a 1-bit adder according to Fig. 2;

Fig. 4, a cell structure of the 1-bit adder according to Fig. 3;

Fig. 5, an 8-bit adder composed according to the cell structure relative to Fig. 1;

Fig. 6, an unprogrammed SUBMACRO X consisting of four cells (analogous to a 1-bit adder relative to Fig. 4, or Fig. 5) with the necessary line connections;

Fig. 7, a partial section of an integrated circuit (chip) with a plurality of cells and a separate SUBMACRO X according to Fig. 6;

Fig. 8, an integrated circuit (chip) with an orthogonal structure of a quasi random plurality of cells and an externally assigned compiler;

Fig. 9, a first exemplary embodiment of a plurality of integrated circuits coupled to form a central processors (data flow processor) according to Fig. 8;

Fig. 10, a second exemplary embodiment of a plurality of integrated circuits coupled to form a central processor (data flow processor) according to Fig. 8;

Figs. 11a-11c an exemplary embodiment of a MACRO for adding two numerical series;

Fig. 12, an exemplary structure of a cell comprising multiplexers for selection of the respective logic modules;

Fig. 13, a synchronizing logic circuit using, e.g., a standard TTL module 74148;

Fig. 14, the cascading of four DFPs, with the connection between I/O pins shown only schematically (actually, a depicted connection means a plurality of lines);

Fig. 15, the homogeneity achieved by cascading;

Fig. 16a, the structure of the I/O cells, with the global connections not taken outside;

Fig. 16b, the structure of the I/O cells, but with the global connections taken outside;

Fig. 17a, the cascading resulting from Fig. 16a, depicting a corner cell and the two driver cells communicating with it, of the cascaded modules (compare with Fig. 14);

Fig. 17b, the cascading resulting from Fig. 16b, depicting a corner cell as well as the two driver cells communicating with it, of the cascaded modules (compare Fig. 14);

Fig. 18a, a multiplication circuit (compare Fig. 11a);

Fig. 18b, the internal structure of the DFP after loading (compare Fig. 11b);

Fig. 18c, a result of multiplication;

Fig. 19a, a cascade circuit, with the adder of Fig. 11 and the multiplier of Fig. 18 wired in series for increased computing capacity;

Figs. 19b and 19c, the operating mode of the DFP in the memory, as well as the states of counters 47, 49;

Fig. 20, the block diagram of a conventional computer;

Fig. 21, the possible structure of the computer of Fig. 20 with the aid of an array of cascaded DFPs;

Fig. 22, a section of a DFP showing the line drivers.--